WhiteRabbit for ArrayTrig & Timing

- First WR-light: Cerenkov shower detection lacksquare
- **Digital trigger**
- Longterm tests



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WR: The Basic Elements

WR Master: WR Switch





Figure 1: The White Rabbit network

NB: Performs as a "normal Eth-Network" non-WR components.



White Rabbit at CTA: Baseline architecture



White Rabbit at CTA: Baseline architecture



White Rabbit (WR) - Executive summary (1)

- Basic Tests, as reported earlier (since spring 2012):
 - Clock Stability is proven to be excellent in Laboratory + Field-installation: rms<200ps</p>
 - **TriggerTime stamping** with **1ns precision** is implemented, verified + stable.
 - See CTA-meetings @ Amsterdam, Rom, Chicago



These results were shown first in Oct 2012...

For details please refer to three ICRC-2013 paper (ID1146, ID1153, ID1164)



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Figure 5: Laboratory-Measurement: Distribution of time difference between PPS clock pulses from SPEC1 and

White Rabbit (WR) - Executive summary (2)

WhiteRabbit is now also used to trigger on AnalogSum (4x HiSCORE PMs)

- Digital trigger extended to new functionality
- Demonstrates flexibility of the (standard) "WR user interface"



inside the SPEC :

Figure 3: The modified FPGA architecture of the SPEC card for timestamping and evaluating incoming signals. The left side shows an incoming signal and the resulting output trigger signal after a constant delay of 40 ns.

PS out SFP

SPEC card

Timestamp

UDP pake

8 Bit / 125 MHz

FPGA

White Rabbit

fabric

If 9 contiguous '1' in 16 Bits (eq. 9 ns) the

FIFO

1ns accurate tric

WR fiber link

LM32

CPU

White Rabbit - Executive summary (3)

Longterm-tests @ DESY-Environmental Chamber

- DESY environmental-chamber (CTA-mirror tests); April/May, 2013: ~10 days of tests
- Temperature -20C ... +40C 2-3 days cycles → FiberCable 500m
- 0C ... +30C 2-3 days cycles → WR-Node (the camera card)
- No measureable temperature effects observed
 - → Trigger-stamps : +-1ns → rms<0.5ns
 - → Phase of 1 PPS-references : rms < 200ps</p>





Figure 4: Experimental Setup (baseline configuration). WR fibers are 20 m long to SPEC1 and 520 m to SPEC2. For tests in the environmental chamber, the 500 m WR-fiber and/or the SPEC2 card are located in the DESY-climate chamber.

White Rabbit - Executive summary (4)

- > Network structure
- > Tests-A: single WR-Switch (max. 17 Telescopes) → OK
- > Tests-B: two-level WR's 17x17 = 289 Telescopes



GPS

clock

White Rabbit

Switch

White Rabbit

Master

White Rabbit

node

White Rabbit - Performance Overview

White Rabbit is a long-term CERN project, well supported and very advanced.

> WR: verified by DESY @Lab & @HiSCORE & by an active community (rapidly growing)

- Eg. LHAASO-plan: >>1000 WR installations soon.
- > Industrial Support @ 5 countries, >5 companies; off-the-shelve; OpenHard/SoftwareProject !!!
- > Ethernet-standard (PTP-extension, pending) → the future of TimeSync

> Main WR-Architecture principles:

- Ethernet Network architecture (redundant ! flexible, no limits)
- One single Fiber for synchronization & Gbps-ethernet
- Absolute clocks at each telescopes: fully correct at any time
- Time stamping @ telescopes locally with full time precision
- Camera-Interface with MezzanineCard

Adaptation to any Camera-Interface is easy; documented

- Extra-feature: Test pulse generation at camera with (sub-)nsec precision !
 - In all Telescopes synchronously !
 - Any complicated time-series and topological pulses per telescope are possible.

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 - In all Telescopes synchronously !
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compare: to MUTIN project (current design)

- center → point ("star")
- Two fibers per telescope
- absolute clock at center (calibration)
- at center only
- standard interface ?
- proprietary



White Rabbit - To Do

Ready :

Standard Camera time-synchronization & stamping

To be done:

- > Extend the Camera Interfaces:
 - Define IFs, then update the simple (standard) WR mezzanine card
 - LST definition under development
 - MST, SST missing
 - In autumn: test with LST ?

More tests

- So far: Integrated time field tests >100 days, Laboratory / Climate: >20 days
- Additional: compare in Laboratory with MUTIN, still in 2013.
- New: Operate in "full user mode" at a remote site, for realistic verification (used as "black box").
 This should be a required test mode for "service systems" (like timing...)



White Rabbit - Next HiSCORE setup

Plan for October 2013:

> HiSCORE array:

Install the 9 station array with WhiteRabbit (0.1 km2)

A full-scale test (aiming at 50TeV gamma's)







WhiteRabbit @ CTA : possible layout for Array-Timing, TimeStamping & ArrayTrigger



Only a few components are needed:

- per telescope : 1 x WhiteRabbit Node (PCIe) + 1 standard fiber (SM;1390/1510nm)

per array : 1...n WhiteRabbit Switches

Conclusion

- > WR is proven and ready to go.
 - In routine operation: 1-ns-precision, RMS < 0.2ns,
- > Is a new Ethernet standard (PPT-extension)
- > Excellent performance, reliability, guaranteed support, and flexibility
- It does
 - -- time synchronization & trigger time stamping and
 - -- calibration pulse generation @ sub-nsec precision (at each telescope sites) !!











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White Rabbit for CTA?

> January 2012:

"WR looks like a good candidate for (sub)nsec time synchronization in CTA"

April 2013:

In practice - WhiteRabbit is doing (sub)nsec time synchronization in HiSCORE. rms<200ps ! and surely top-candidate for CTA !

> A typical WR-user needs to

- 1. Acquire WR-hardware all basic modules commercially
- 2. Application specific firmware (if needed)
- 3. Verify calibration and get some experience ... and use it
- \rightarrow Almost out-of-the-box
- > Array Trigger distribution: (time stamps to AT-unit) comes naturally with the architecture;

is a nice "Add-on feature" of a fully ethernet based system

- > Evaluation schedule: we suggest early summer (Paris or Zeuthen) MUTIN: @LabTests -cross-verification wrt WR is welcome
- > References:
 - CTA-Rome Consortium meeting, Oct.2012: R.Wischnewski/M.Brueckner
 https://www.cta-observatory.org/indico/materialDisplay.py?contribId=157&sess
 ionId=19&materialId=slides&confId=...
 - CTA-ACTL meeting, June.2012/Feb.2013: R.Wischnewski/M.Brueckner
 - 6th WhiteRabbit-Workshop, March-2012, GSI R.Wischnewski/M.Brueckner
 - 7th WhiteRabbit-Workshop, November-2012, Madrid M.Brueckner/R.Wischnewski <u>http://www.ohwr.org/projects/white-rabbit/white-rabbit/wiki/Nov2012/Meeting</u>

WR – Tunka Results (an example)

> Test 1:Loopback Fiber (2x1km) WRS-SPEC: check Clock-offset by 1PPS pulse

Clock-offset = T_SPEC – T_WRS (5 GHz DRS4)

ITTPPS (LoopBack SPEC-WRS)





The fiber delay, induced by ambient temperature variation, are compensated by WR to < 0.2 ns level

White Rabbit

- > White Rabbit is a fully deterministic Ethernet-based network (Gbit standard) for
 - time synchronization with precision: 1nsec/ phase stability <0.1ns</p>
 - data transfer
- > It can synchronize over 1000 nodes with sub-ns accuracy over fiber lengths > 10 km.
 - Developed at CERN
 - Plans for LHC-upgrade, GSI-Accelerator complex (FAIR), CTA, km3net, LHHASO
 - Big community, all open source (software, fpga designs, pcb schematics and layouts)
 - Gigabit-Ethernet is used
 - DESY is active WR-developer since 2/2012
 - HiSCORE is the first real application
 - Implementing WR- into Ethernet standard coming soon



Ralf Wischnewsk

WR – setup in Tunka

White Rabbit Installation with a maximum of redundant cross-calibration options (October 2012 - today):

> 2km loopback fiber cable connected to DRS4 to compare WRS and SPEC (2km) PPS clocks

> Crosswise PPS->TDC connection to test TDC and White Rabbit

- 2x SPEC within HiS1 station
- 2x SPEC in 2 stations (HiS4 + Tunka-1)

> Loopback PPS connection to test TDC performance (HiS 3)





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HiSCORE setup overview (Oct.2012 comissioned)



HiSCORE setup overview





- DRS4 as 5 GHz "digital scope"
- Raspberry Pi transports
 - USB Terminal

. . .

- DRS4 (Domino Ring Sampler)
- Temperature sensor



Б

DAQ center

HiSCORE setup



• PPS signals (DIO output 1) connected to TDC-inputs (DIO input 3)



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Results - 2 km fiber loopback with DRS4





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WR – Lab. test



WR-Link

1 PPS timing

(DRS4 5GS/s)

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> Setup:

- Two WR-SPEC cards: Mster-Slave WR-link + fiber
- > Time test:
 - Comparing the master/slave 1-PPS outpu Clock-offset = T_SPEC T_WRS

