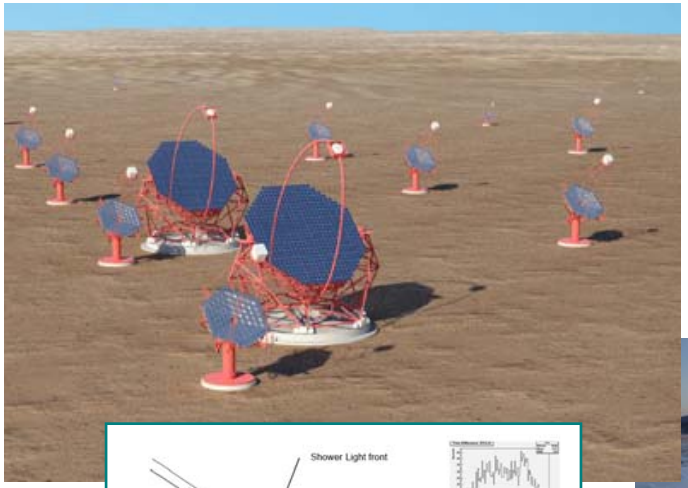
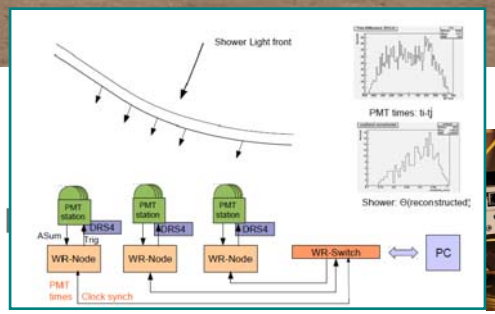
CTA-WhiteRabbit - an update.

- **First WR-light: Cerenkov shower detection**
- **Digital trigger**
- **Longterm tests**





Ralf Wischnewski (DESY)
Martin Brueckner (HumboldtUniv Berlin)

Chicago , 20130529
TriggerWG SeeVogh, 20130523

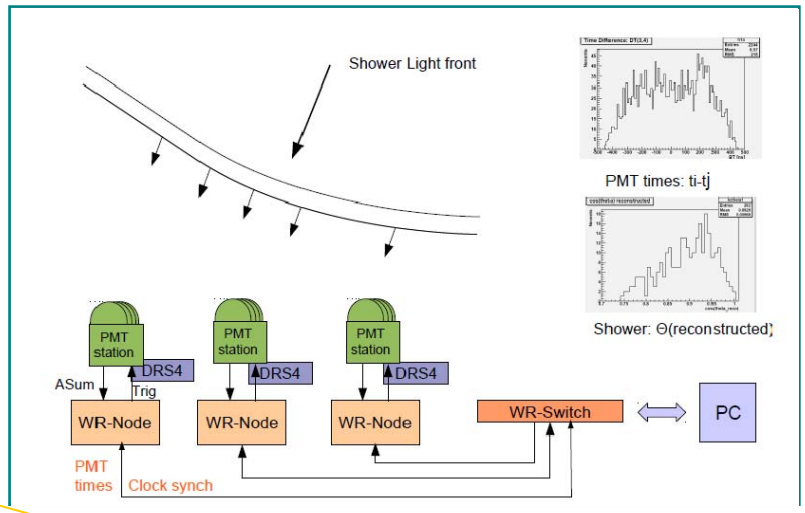
White Rabbit (WR) - Executive summary (1)

> We had reported before (since spring 2012):

- Clock Stability is proven to be excellent in Laboratory / Field-installation: rms<200ps
- TriggerTime stamping with 1ns precision implemented / verified. Stable.

> WhiteRabbit is now also used to trigger on AnalogSum (4x HiSCORE PMs)

- Digital trigger extended to new functionality
- Demonstrates flexibility of the (standard) ”WR user interface”



“First WR Cerenkov light”

HiSCORE prototype installation:
Sketch of the Array-Timing and DAQ (DRS4 boards) system.

The WR-nodes (at each station / telescope) act as digital AnalogSumTrigger and time-stamping units. Based only on the ns-trigger times (upper plot), a preliminary shower direction reconstruction was done (plane wave, lower plot; DRS4-waveforms are used in full analysis).
This demonstrates capability and flexibility of the WR-node cards; that goes far beyond time synchronization.

White Rabbit - Executive summary (2)

- Longterm-tests @ DESY-Environmental Chamber completed
  - DESY environmental-chamber (CTA-mirror tests); April/May, 2013: ~10 days of tests
  - Temperature -20C … +40C 2-3 days cycles - Fiber 500m
  - 0C … +30C 2-3 days cycles - WR-Node (the camera card)
  - No measureable temperature effects observed
    - → Trigger-stamps : +-1ns → rms<0.5ns
    - → Phase of 1 PPS-references : rms < 200ps

- To be done:
- Standard Camera time-synchronization & stamping: READY TO GO.
- Complex Camera Interfaces: define IFs and build one mezzanine card
  - LST – definition under development
  - MST, SST - missing
  - In autumn: test with LST

White Rabbit - Performance Overview

White Rabbit is a long-term CERN project, well supported and very advanced.

> **WR: verified by DESY @Lab & @HiSCORE & by an active community (rapidly growing)**
  - Eg. LHAASO-plan: >>1000 WR installations soon.
> **Industrial Support** @ 5 countries, >5 companies; off-the-shelve; OpenHard/SoftwareProject !!!
> **Ethernet-standard** (PTP-extension, pending) → the future of TimeSync

> **Main WR-Architecture principles:**

- **Ethernet Network** architecture (redundant ! flexible, no limits)
- **One single Fiber** for synchronization & Gbps-ethernet
- **Absolute clocks at each telescopes**: fully correct at any time
- **Time stamping** @ telescopes locally with full time precision
- **Camera-Interface with MezzanineCard**

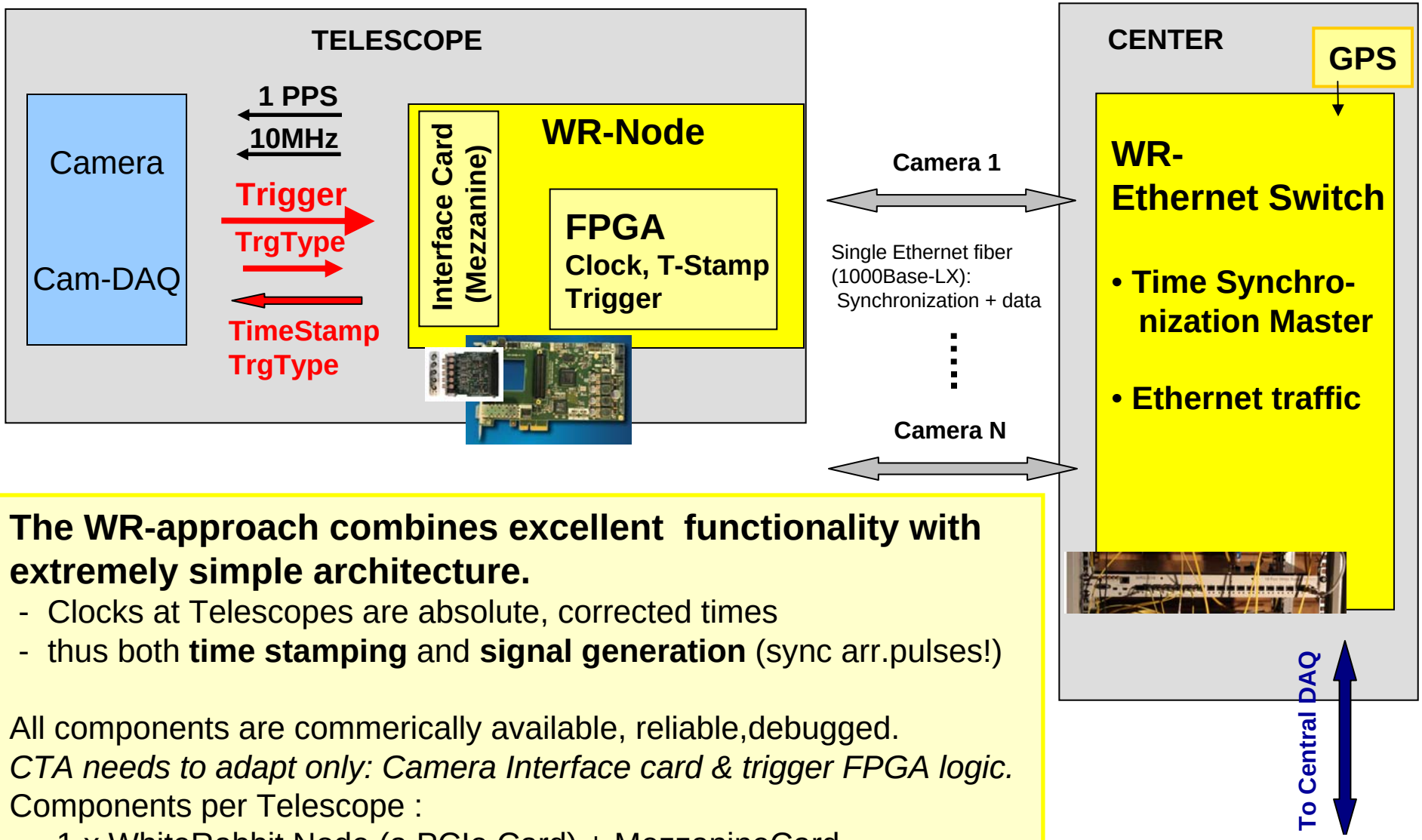
  Adaptation to any Camera-Interface is easy; documented

- **Extra-feature: Test pulse generation at camera** with (sub-)nsec precision !
  - In all Telescopes synchronously !
  - Any complicated time-series and topological pulses per telescope are possible.

compare: to MUTIN project (current design)

- center→point ("star")
- Two fibers per telescope
- absolute clock at center (calibration)
- at center only
- standard interface ?
- proprietary
- Not available

White Rabbit at CTA: Baseline architecture



The WR-approach combines excellent functionality with extremely simple architecture.

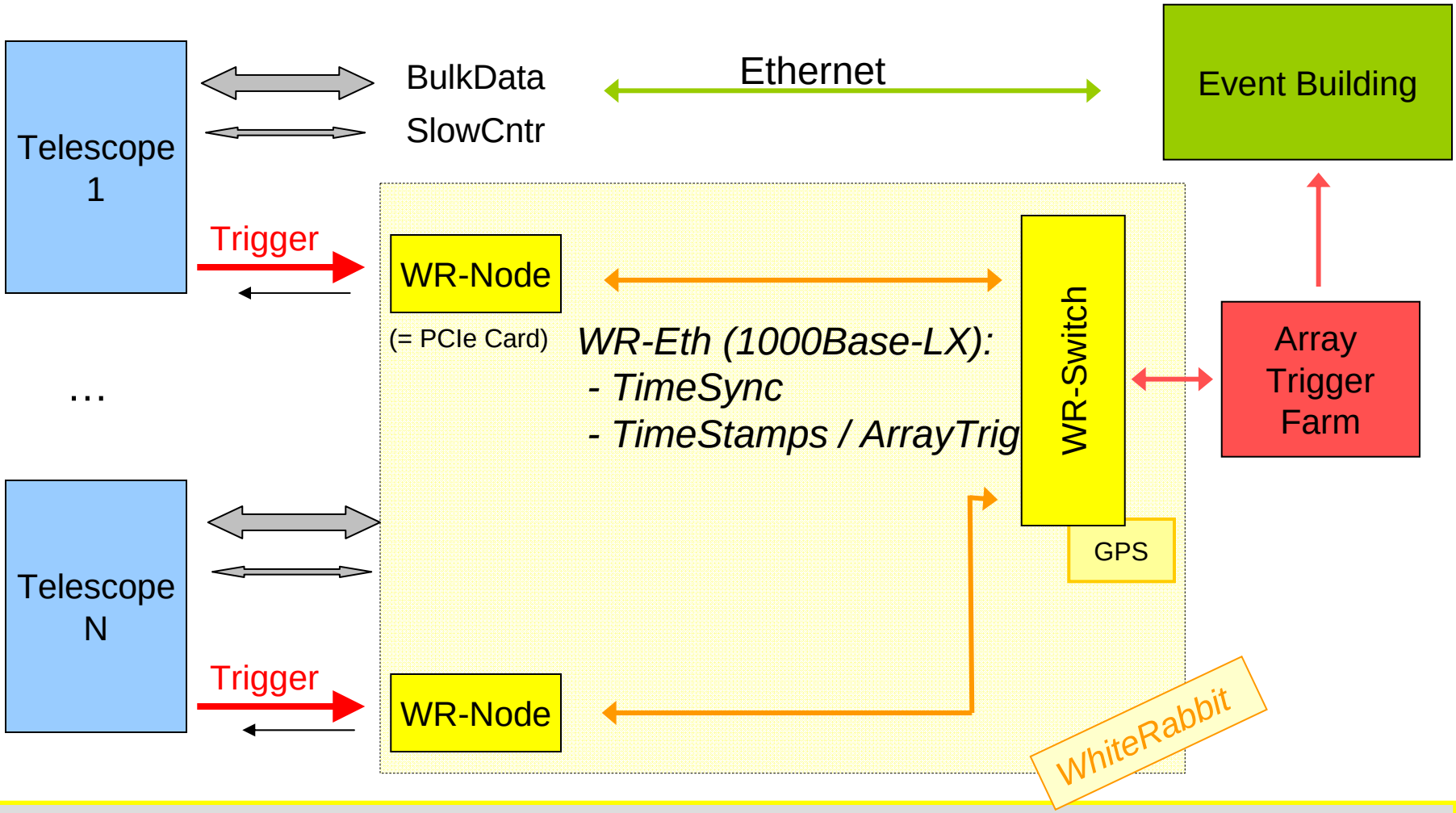
- Clocks at Telescopes are absolute, corrected times
- thus both **time stamping** and **signal generation** (sync arr.pulses!)

All components are commerically available, reliable,debugged.
CTA needs to adapt only: Camera Interface card & trigger FPGA logic.
Components per Telescope :

- 1 x WhiteRabbit Node (a PCIe Card) + MezzanineCard
- 1 standard fiber (SM;1390/1510nm)

Per Array : WhiteRabbit Switches (Nb.of.Telescopes / 18).

WhiteRabbit @ CTA : possible layout for Array-Timing, TimeStamping & ArrayTrigger



Only a few components are needed:

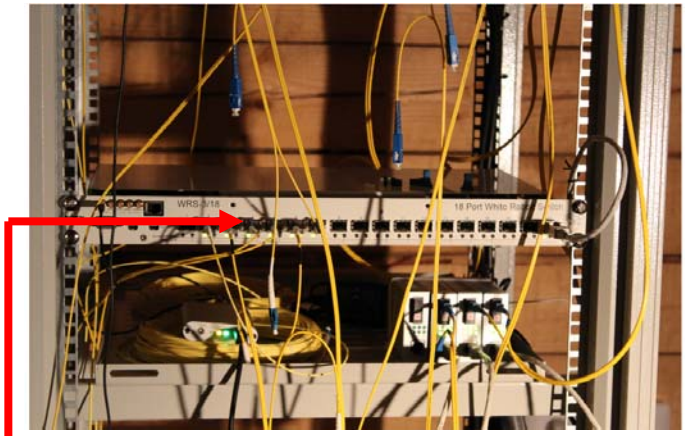
- per telescope : 1 x WhiteRabbit Node (PCIe) + 1 standard fiber (SM;1390/1510nm)
- per array : 1…n WhiteRabbit Switches

> Stop here, for the short update.

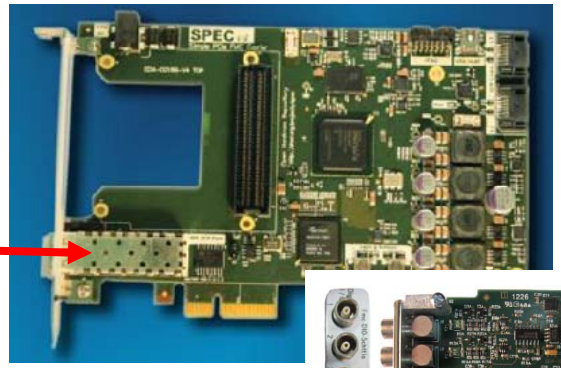
> A few more slides on detailed performance tests (partially already known).

WR : Basic Elements

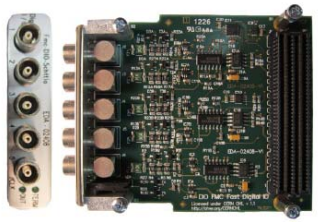
WR Switch



1Gbit fiber



SPEC card



FMC 5ch DIO card

- WR-Switch
  - Can work as WR Master
  - 18 SFP-slots, 1Gbit/s Ethernet each
  - GPS clock port
- SPEC card: universal WR node
  - FMC mezzanine, PCIe and USB connector
  - Master and slave mode
- FMC mezzanine card
  - General i/o mezzanine (5 LEMO ports), programmable thresh.
  - Suitable for trigger latching and 1PPS time calibration

The DESY modified WR setup for HiSCORE

- Trigger Time Latching
- 1ns-TDC implemented on FPGA
- Digital Trigger for Analog PMTSum
- Various output calibration pulses (PPS, ….)

(status 04/2013)

Conclusion

> WR is proven and ready to go.

> Is the new Ethernet standard (PPT-extension)

> Excellent performance, reliability, guaranteed support, and flexibility

> It does

-- time synchronization & trigger time stamping

and

-- calibration pulse generation @ sub-nsec precision (at each telescope) !!

> Thank you

> BACKUP SLIDES

White Rabbit for CTA ?

> January 2012:

"WR looks like a good candidate for (sub)nsec time synchronization in CTA"

April 2013:

In practice - WhiteRabbit is doing (sub)nsec time synchronization in HiSCORE. rms<200ps !

and surely top-candidate for CTA !

> A typical WR-user needs to

1. Acquire WR-hardware - all basic modules commercially
2. Application specific firmware (if needed)
3. Verify calibration and get some experience … and use it

→ Almost out-of-the-box

> Array Trigger distribution: (time stamps to AT-unit) comes naturally with the architecture;

is a nice "Add-on feature" of a fully ethernet based system

> Evaluation schedule: we suggest early summer (Paris or Zeuthen)

MUTIN: @LabTests -cross-verification wrt WR is welcome

> References:

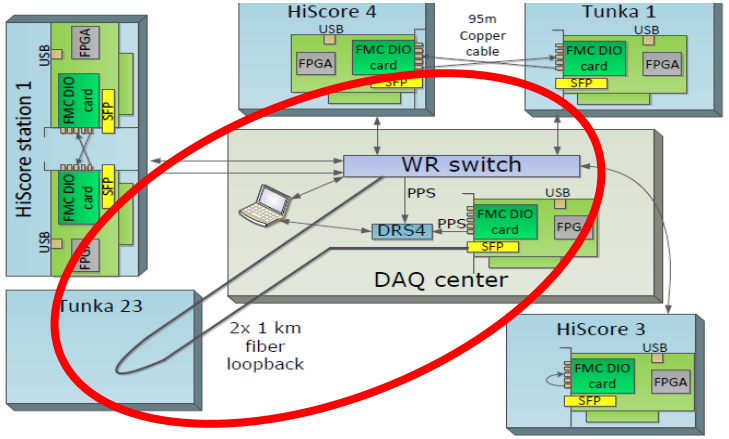
- CTA-Rome Consortium meeting, Oct.2012: R.Wischnewski/M.Brueckner

  https://www.cta-observatory.org/indico/materialDisplay.py?contribId=157&sessionId=19&materialId=slides&confId=…
- CTA-ACTL meeting, June.2012/Feb.2013: R.Wischnewski/M.Brueckner
- 6th WhiteRabbit-Workshop, March-2012, GSI R.Wischnewski/M.Brueckner
- 7th WhiteRabbit-Workshop, November-2012, Madrid M.Brueckner/R.Wischnewski

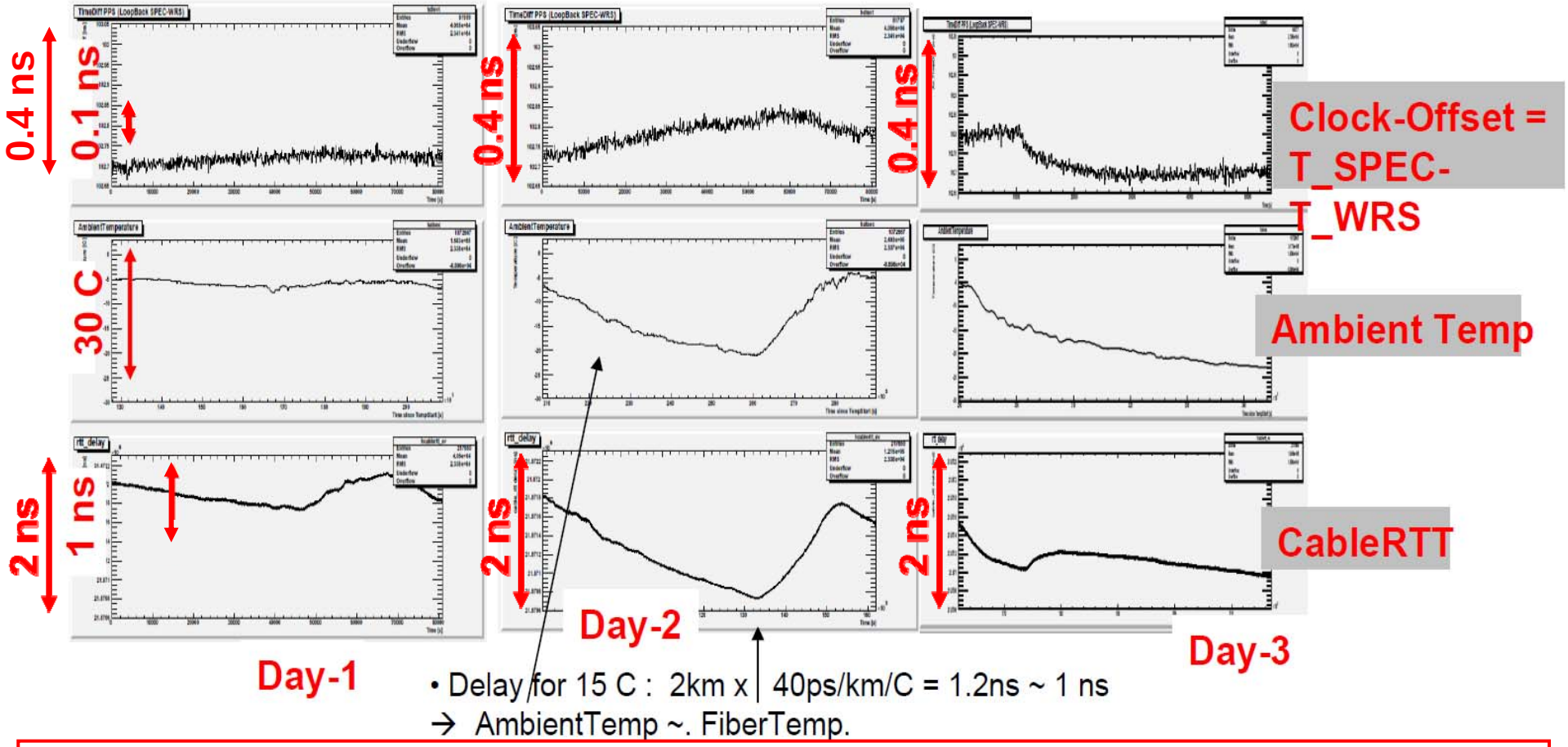
  http://www.ohwr.org/projects/white-rabbit/white-rabbit/wiki/Nov2012/Meeting

WR – Tunka Results (an example)

- **Test 1:Loopback Fiber (2x1km) WRS-SPEC: check Clock-offset by 1PPS pulse**



Clock-offset = T_SPEC – T_WRS (5 GHz DRS4)

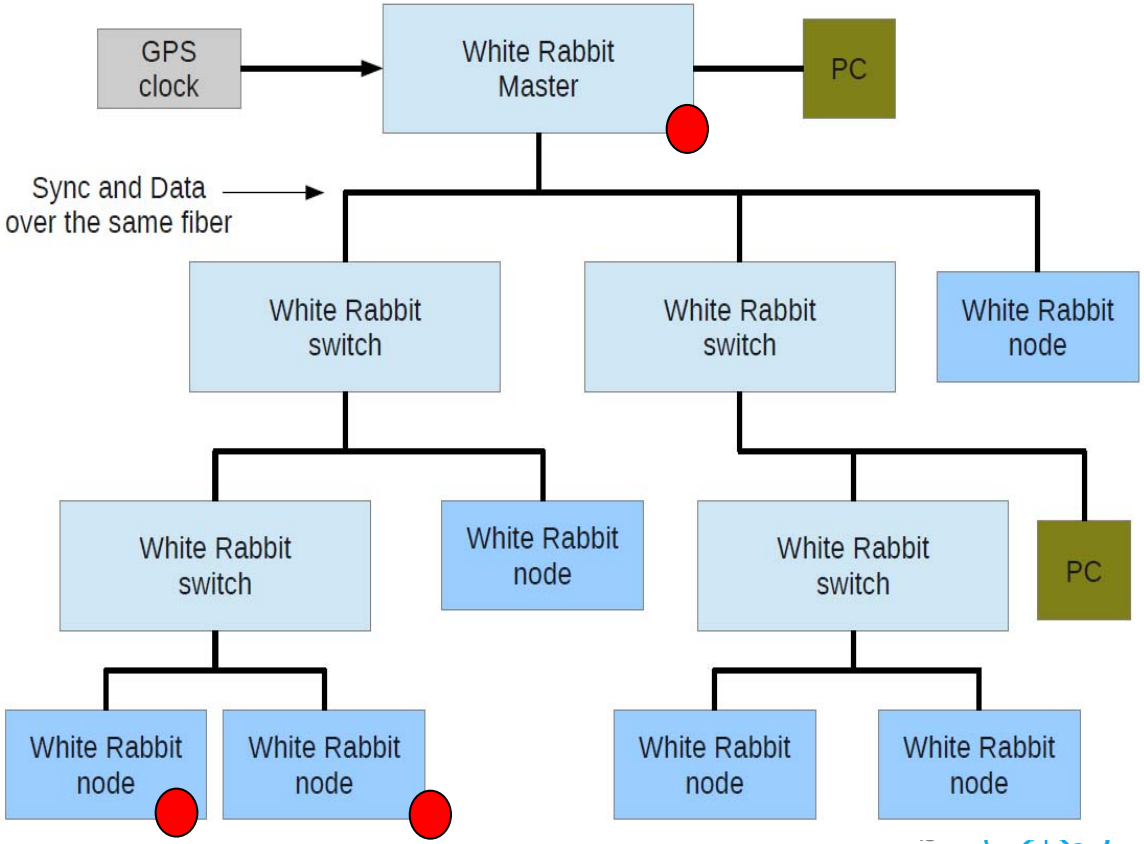


The fiber delay, induced by ambient temperature variation, are compensated by WR to < 0.2 ns level

White Rabbit

- White Rabbit is a fully deterministic Ethernet-based network (Gbit standard) for
  - time synchronization with precision: 1nsec/ phase stability <0.1ns
  - data transfer
- It can synchronize over 1000 nodes with sub-ns accuracy over fiber lengths > 10 km.

- Developed at CERN
- Plans for LHC-upgrade, GSI-Accelerator complex (FAIR), CTA, km3net, LHHASO
- Big community, all open source (software, fpga designs, pcb schematics and layouts)
- Gigabit-Ethernet is used
- DESY is active WR-developer since 2/2012
- HiSCORE is the first real application
- Implementing WR- into Ethernet standard coming soon



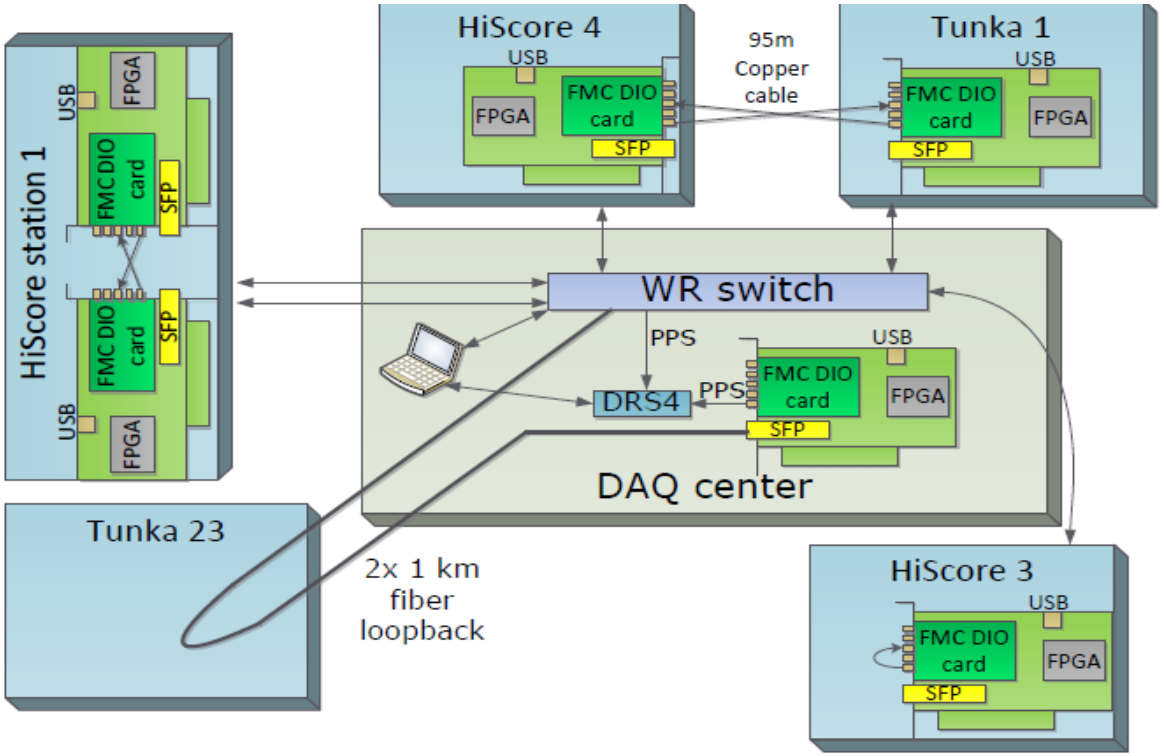
WR – setup in Tunka

White Rabbit Installation with a maximum of redundant cross-calibration options (October 2012 - today):

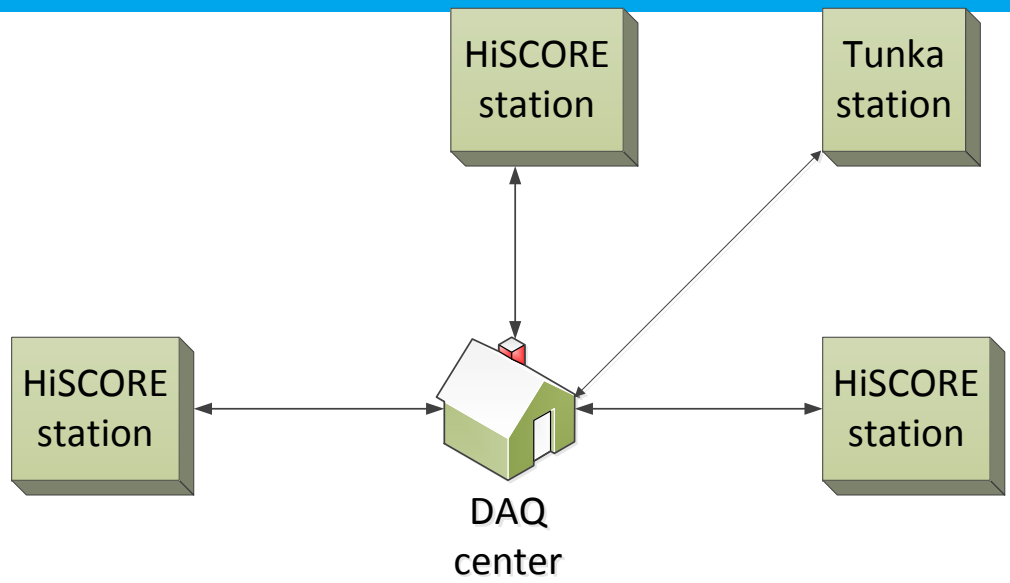
> **2km loopback fiber cable connected to DRS4 to compare WRS and SPEC (2km) PPS clocks**

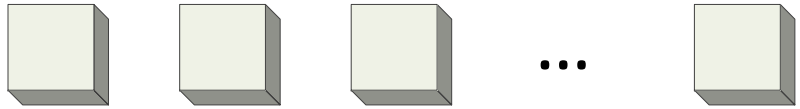
> **Crosswise PPS->TDC connection to test TDC and White Rabbit**
- **2x SPEC within HiS1 station**
- **2x SPEC in 2 stations (HiS4 + Tunka-1)**

> **Loopback PPS connection to test TDC performance (HiS 3)**



HiSCORE setup overview (Oct.2012 comissioned)

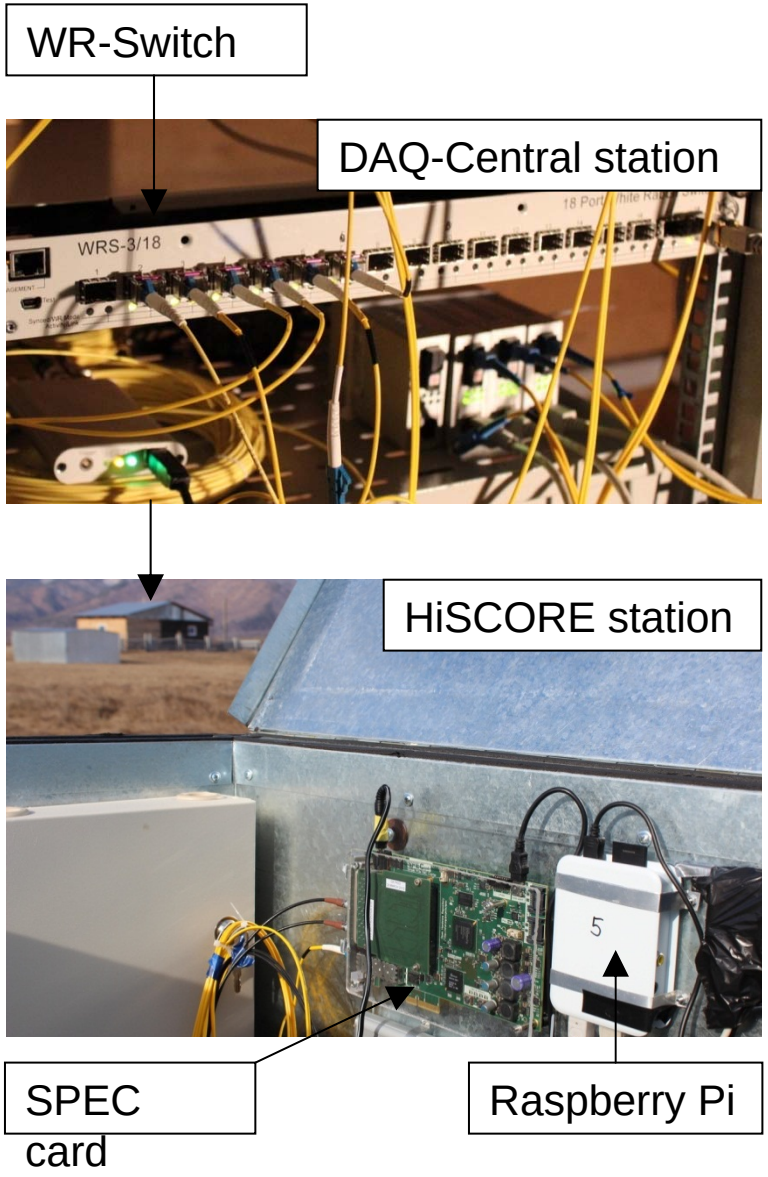


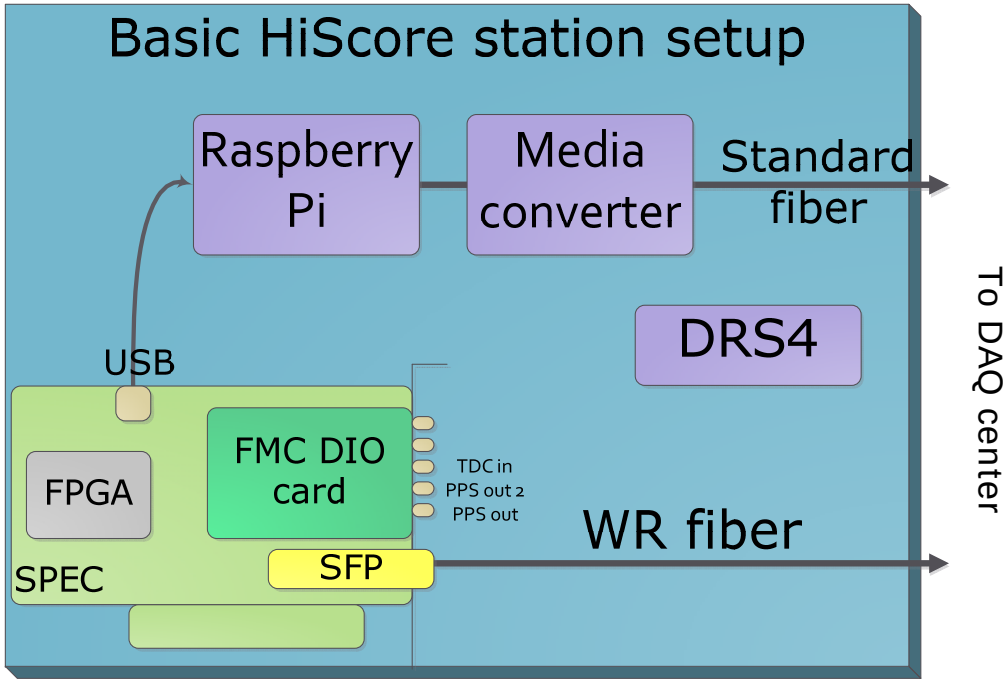


More HiSCORE stations in future

- 1 km² in 2013/14 : 20-40 stations
- 100 km²: > 2000 stations

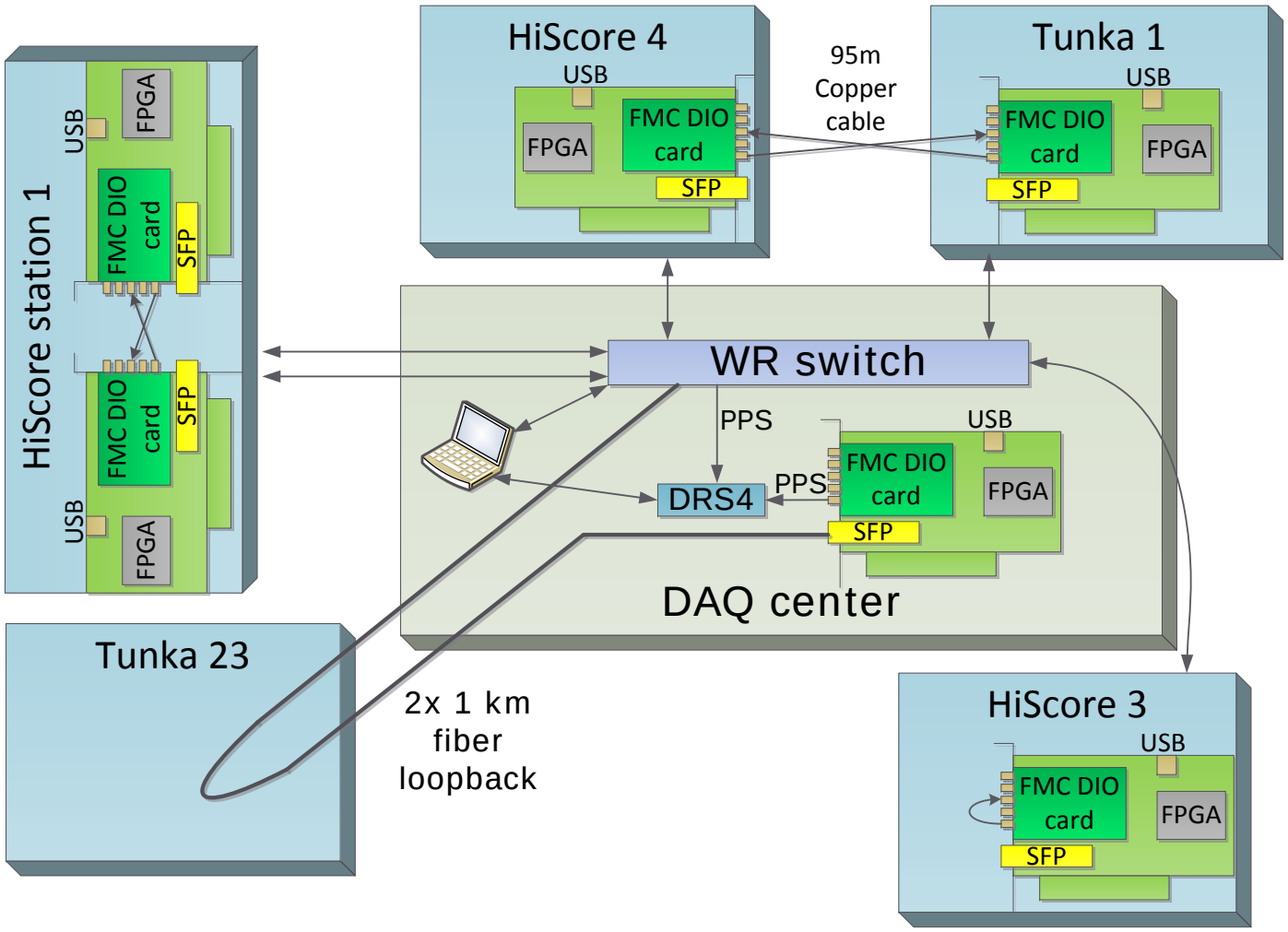
HiSCORE setup overview





- DRS4 as 5 GHz “digital scope”
- Raspberry Pi transports
  - USB Terminal
  - DRS4 (Domino Ring Sampler)
  - Temperature sensor
  - …

HiSCORE setup



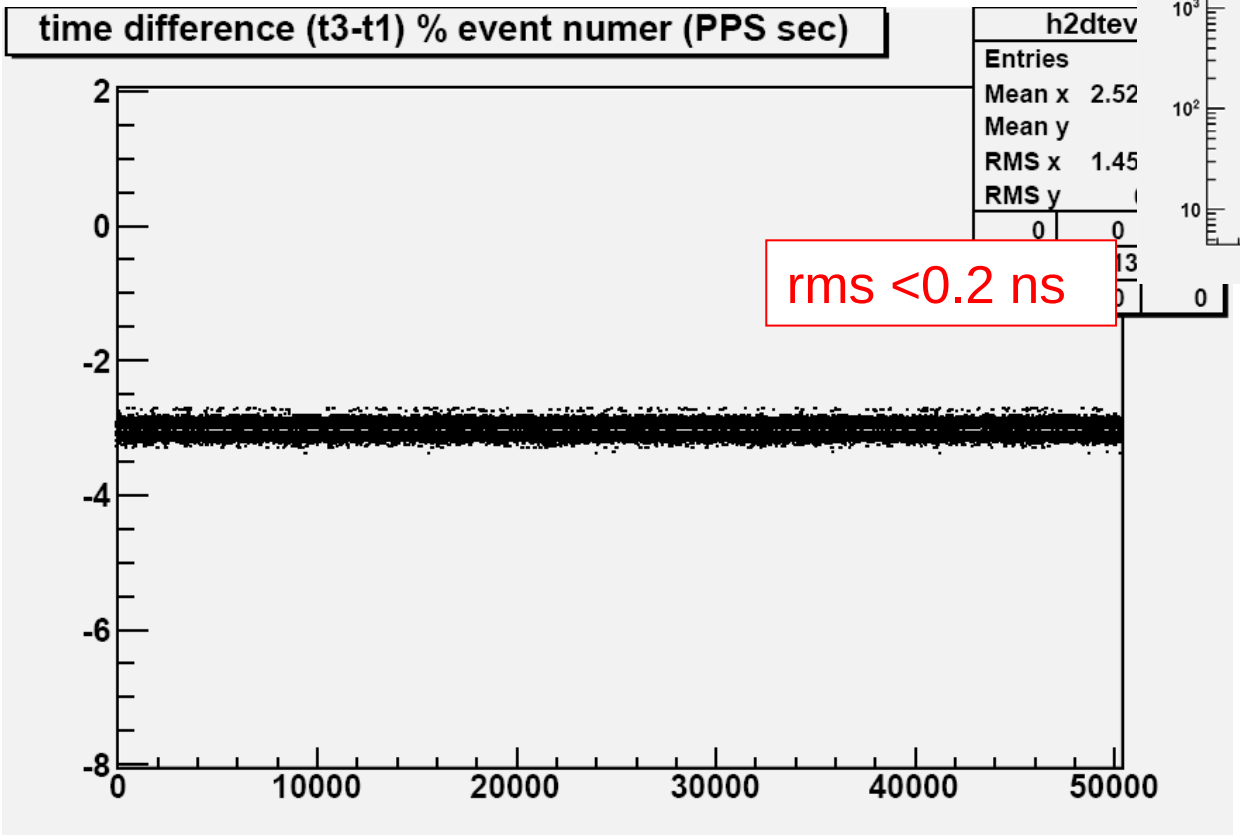
- PPS signals (DIO output 1) connected to TDC-inputs (DIO input 3)

Results - 2 km fiber loopback with DRS4

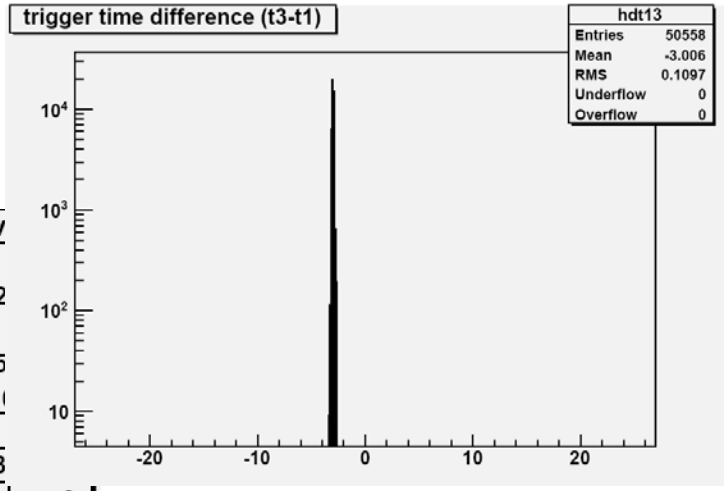
1. Test :

LoopBack Fiber over 2x1km
back to Laboratory

(5GHz DRS4-measurement)

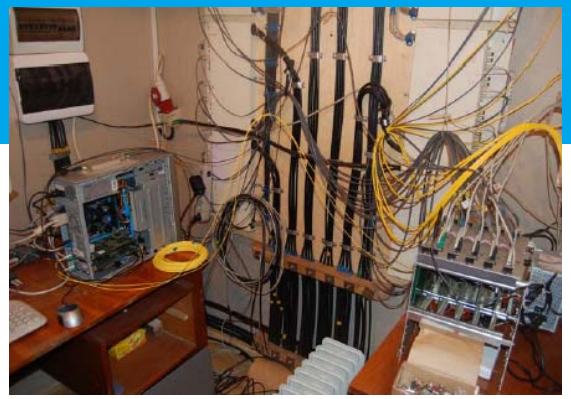


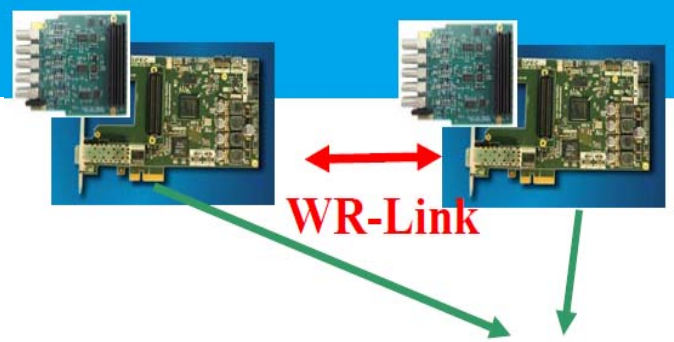
rms <0.2 ns



14hr run

WR – Lab. test





1 PPS timing
(DRS4 5GS/s)

- **Setup:**
  - **Two WR-SPEC cards: Mster-Slave WR-link + fiber**
- **Time test:**
  - **Comparing the master/slave 1-PPS outpu**

Clock-offset = T_SPEC – T_WRS